

WHAT IS CLAIMED IS:

- 1 1. A logic circuit, comprising:
2 a first logic stage comprising first logic circuitry operable to receive a first
3 set of input signals and to generate a first output signal in response
4 thereto, wherein said first logic circuitry comprises clocked
5 precharge and evaluate transistors and further comprises full-
6 complementary low-beta-ratio static logic; and
7 at least one subsequent logic stage, comprising second logic circuitry
8 operable to receive a second set of input signals and to generate a
9 second output signal in response thereto, wherein said second logic
10 circuitry comprises non-clocked, low-beta-ratio static logic.

- 1 2. The logic circuit of claim 1, wherein said first logic circuitry comprises a
2 plurality of input transistors configured in a first tapered stack.

- 1 3. The logic circuit of claim 2, wherein said clocked precharge circuitry
2 comprises at least one pMOS transistor operable to hold a first node at a voltage, V_{dd} ,
3 during a precharge phase.

- 1 4. The logic circuit of claim 3, wherein said tapered stack of input transistors
2 comprises a plurality of nMOS transistors operable to conditionally pull said first node to
3 a lower voltage during an evaluation phase in response to a predetermined set of input
4 signals.

1 5. The logic circuit of claim 4, wherein said subsequent logic stage
2 comprises a plurality of input transistors configured in a second tapered stack connected
3 to a second node that is maintained at a voltage, Vdd, during a precharge phase and
4 wherein said input transistors are operable to conditionally pull said node to a lower
5 voltage during an evaluation phase in response to a predetermined set of input signals.

1 6. The logic circuit of claim 5, wherein said low-beta-ratio static logic in said
2 second logic circuitry comprises a plurality of pMOS transistors operably connected to
3 said second node and wherein said plurality of pMOS transistors are operable to hold said
4 second node at a voltage, Vdd, during said precharge phase.

1 7. The logic circuit of claim 6, wherein said second tapered stack of input
2 transistors comprises a plurality of nMOS transistors with each individual nMOS
3 transistor in said second stack has its gate connected to the gate of one of said plurality of
4 pMOS transistors.

1 8. The logic circuit of claim 7, wherein the beta-ratio of said non-clocked
2 static logic in said second logic circuitry is less than 1:1.

1 9. The logic circuit of claim 8, wherein the precharge load for maintaining
2 said second node at Vdd is distributed across said plurality of pMOS transistors
3 connected to said second node.

4 10. A method of operating a logic circuit, comprising:
 5 receiving a first set of input signals in a first logic circuit and generating a
 6 first output signal in response thereto,
 7 receiving a second set of input signals in a second logic circuit and
 8 generating a second output signal in response thereto,
 9 wherein said first logic circuitry comprises clocked precharge and evaluate
 10 transistors and further comprises full-complementary low-beta-
 11 ratio static logic; and
 12 wherein said second logic circuitry comprises non-clocked, low-beta-ratio
 13 static logic.

1 11. The method of claim 10, wherein said first logic circuitry comprises a
 2 plurality of input transistors configured in a first tapered stack.

1 12. The method of claim 11, wherein said clocked precharge circuitry
 2 comprises at least one pMOS transistor operable to hold a first node at a voltage, Vdd,
 3 during a precharge phase.

1 13. The method of claim 12, wherein said tapered stack of input transistors
 2 comprises a plurality of nMOS transistors operable to conditionally pull said first node to
 3 a lower voltage during an evaluation phase in response to a predetermined set of input
 4 signals.

1 14. The method of claim 13, wherein said subsequent logic stage comprises a
2 plurality of input transistors configured in a second tapered stack and wherein said
3 second tapered stack of input transistors is connected to a second node that is maintained
4 at a voltage, Vdd, during a precharge phase and wherein said input transistors are
5 operable to conditionally pull said node to a lower voltage during an evaluation phase in
6 response to a predetermined set of input signals.

1 15. The method of claim 14, wherein said low-beta-ratio static logic in said
2 second logic circuitry comprises a plurality of pMOS transistors connected to said second
3 node and wherein said plurality of pMOS transistors are operable to hold said second
4 node at a voltage, Vdd, during said precharge phase.

1 16. The method of claim 15, wherein said second tapered stack of input
2 transistors comprises a plurality of nMOS transistors with each individual nMOS
3 transistor in said second stack has its gate connected to the gate of one of said plurality of
4 pMOS transistors.

1 17. The method of claim 16, wherein the beta-ratio of said non-clocked static
2 logic in said second logic circuitry is less than 1:1.

1 18. The method of claim 17, wherein the input transistors in said second
2 tapered stack in said second logic circuitry, wherein said clocked precharge circuitry
3 comprises at least one pMOS transistor operable to hold a first node at a voltage, Vdd,
4 during an evaluation phase.